



IEC 62433-2

Edition 1.0 2008-10

# INTERNATIONAL STANDARD

---

**EMC IC modelling –  
Part 2: Models of integrated circuits for EMI behavioural simulation – Conducted  
emissions modelling (ICEM-CE)**

INTERNATIONAL  
ELECTROTECHNICAL  
COMMISSION

PRICE CODE



ICS 31.200

ISBN 2-8318-1002-7

## CONTENTS

FOREWORD.....	5
1 Scope.....	7
2 Normative references .....	7
3 Terms and definitions .....	7
4 Philosophy .....	8
4.1 General.....	8
4.2 Conducted emission from core activity (digital culprit) .....	8
4.3 Conducted emission from I/O activity.....	9
5 Basic components .....	9
5.1 General.....	9
5.2 Internal Activity (IA).....	9
5.3 Passive Distribution Network (PDN) .....	10
6 IC macro-models .....	12
6.1 General.....	12
6.2 General IC macro-model .....	12
6.3 Block-based IC macro-model.....	13
6.3.1 Block component.....	13
6.3.2 Inter-Block Coupling component (IBC) .....	14
6.3.3 Block-based IC macro-model structure .....	15
6.4 Sub-model-based IC macro-model .....	17
6.4.1 Sub-model component.....	17
6.4.2 Sub-model-based IC macro-model structure .....	18
7 Requirements for parameter extraction.....	19
7.1 General.....	19
7.2 Environmental extraction constraints .....	19
7.3 IA parameter extraction .....	19
7.4 PDN parameter extraction .....	19
7.5 IBC parameter extraction.....	19
Annex A (informative) Model parameter generation.....	20
Annex B (informative) Decoupling capacitors optimization .....	38
Annex C (informative) Conducted emission prediction.....	40
Annex D (informative) Conducted emission prediction at PCB level .....	41
Bibliography.....	43
Figure 1 – Decomposition example of a digital IC for conducted emissions analysis .....	8
Figure 2 – IA component.....	9
Figure 3 – Example of IA characteristics in time domain .....	10
Figure 4 – Example of IA characteristics in frequency domain.....	10
Figure 5 – Example of a four-terminal PDN using lumped elements .....	11
Figure 6 – Example of a seven-terminal PDN using distributed elements .....	11
Figure 7 – Example of a twelve-terminal PDN using matrix representation .....	12
Figure 8 – General IC macro-model .....	13
Figure 9 – Example of block component.....	13
Figure 10 – Example of block components for I/Os .....	14

Figure 11 – Example of IBC with two internal terminals .....	15
Figure 12 – Relationship between blocks and IBC .....	15
Figure 13 – Block-based IC macro-model .....	16
Figure 14 – Example of block-based IC macro-model .....	17
Figure 15 – Example of simple sub-model .....	18
Figure 16 – Sub-model-based IC macro-model .....	18
Figure A.1 – Typical characterization current gate schematic .....	22
Figure A.2 – Current peak during switching transition .....	22
Figure A.3 – Example of IA extraction procedure from design .....	23
Figure A.4 – Technology Influence .....	23
Figure A.5 – Final current waveform for a program period .....	24
Figure A.6 – Comparison between measurement and simulation .....	24
Figure A.7 – Lumped element model of a package .....	25
Figure A.8 – Circuit structure of the netlist .....	26
Figure A.9 – Principle of the IA computation .....	27
Figure A.10 – Process involved to model $i_A(t)$ .....	27
Figure A.11 – $i_{Ext}(t)$ measured using IEC 61967-4 .....	28
Figure A.12 – $i_A(t)$ and $i_{Ext}(t)$ profiles .....	28
Figure A.13 – Example of a hardware set-up used to extract the PDN parameters .....	30
Figure A.14 – Miniature 50 $\Omega$ coaxial connectors .....	30
Figure A.15 – Impedance probe using two miniature coaxial connectors .....	31
Figure A.16 – Open and short terminations .....	31
Figure A.17 – Measurement probe model .....	31
Figure A.18 – De-embedding principle .....	32
Figure A.19 – Example of a predefined PDN structure .....	33
Figure A.20 – RL configuration .....	34
Figure A.21 – RLC configuration .....	34
Figure A.22 – RLC with magnetic coupling configuration .....	35
Figure A.23 – Impedance seen from Vcc and Gnd .....	35
Figure A.24 – Complete PDN component .....	36
Figure A.25 – Set-up for correlation (left), measurement and prediction (right) .....	37
Figure A.26 – Set-up used to measure the internal decoupling capacitor .....	37
Figure B.1 – Equivalent schematic of the complete electronic system .....	38
Figure B.2 – Impedance prediction and measurements .....	39
Figure C.1 – IEC 61967-4 test set-up standard .....	40
Figure C.2 – Comparison between prediction and measurement .....	40
Figure D.1 – Prediction of the Vdcc noise level at PCB level .....	41
Figure D.2 – Good agreements on the noise envelope .....	42

Table A.1 – Typical parameters for CMOS logic technologies .....	20
Table A.2 – Typical number of logic gates vs. CPU technology .....	21
Table A.3 – R, L and C parameters for various package types .....	21
Table A.4 – Measurement configurations and extracted RLC parameters .....	33

## INTERNATIONAL ELECTROTECHNICAL COMMISSION

**EMC IC MODELLING –****Part 2: Models of integrated circuits for EMI behavioural simulation –  
Conducted emissions modelling (ICEM-CE)**

## FOREWORD

- 1) The International Electrotechnical Commission (IEC) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, IEC publishes International Standards, Technical Specifications, Technical Reports, Publicly Available Specifications (PAS) and Guides (hereafter referred to as "IEC Publication(s)"). Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested IEC National Committees.
- 3) IEC Publications have the form of recommendations for international use and are accepted by IEC National Committees in that sense. While all reasonable efforts are made to ensure that the technical content of IEC Publications is accurate, IEC cannot be held responsible for the way in which they are used or for any misinterpretation by any end user.
- 4) In order to promote international uniformity, IEC National Committees undertake to apply IEC Publications transparently to the maximum extent possible in their national and regional publications. Any divergence between any IEC Publication and the corresponding national or regional publication shall be clearly indicated in the latter.
- 5) IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with an IEC Publication.
- 6) All users should ensure that they have the latest edition of this publication.
- 7) No liability shall attach to IEC or its directors, employees, servants or agents including individual experts and members of its technical committees and IEC National Committees for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication, use of, or reliance upon, this IEC Publication or any other IEC Publications.
- 8) Attention is drawn to the Normative references cited in this publication. Use of the referenced publications is indispensable for the correct application of this publication.
- 9) Attention is drawn to the possibility that some of the elements of this IEC Publication may be the subject of patent rights. IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 62433-2 has been prepared by subcommittee 47A: Integrated circuits, of IEC technical committee 47: Semiconductor devices.

The text of this standard is based on the following documents:

FDIS	Report on voting
47A/794/FDIS	47A/799/RVD

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

A list of all the parts in the IEC 62433 series, under the general title *EMC IC modelling*, can be found on the IEC website.

The committee has decided that the contents of this publication will remain unchanged until the maintenance result date indicated on the IEC web site under "<http://webstore.iec.ch>" in the data related to the specific publication. At this date, the publication will be

- reconfirmed,
- withdrawn,
- replaced by a revised edition, or
- amended.

A bilingual version of this publication may be issued at a later date.

## EMC IC MODELLING –

### Part 2: Models of integrated circuits for EMI behavioural simulation – Conducted emissions modelling (ICEM-CE)

#### 1 Scope

This part of IEC 62433 specifies macro-models for ICs to simulate conducted electromagnetic emissions on a printed circuit board. The model is commonly called Integrated Circuit Emission Model - Conducted Emission (ICEM-CE).

The ICEM-CE model can also be used for modelling an IC-die, a functional block and an Intellectual Property block (IP).

The ICEM-CE model can be used to model both digital and analogue ICs.

Basically, conducted emissions have two origins:

- conducted emissions through power supply terminals and ground reference structures;
- conducted emissions through input/output (I/O) terminals.

The ICEM-CE model addresses those two types of origins in a single approach.

This standard defines structures and components of the macro-model for EMI simulation taking into account the IC's internal activities.

This standard gives general data, which can be implemented in different formats or languages such as IBIS, IMIC, SPICE, VHDL-AMS and Verilog. SPICE is however chosen as default simulation environment to cover all the conducted emissions.

This standard also specifies requirements for information that shall be incorporated in each ICEM-CE model or component part of the model for model circulation, but description syntax is not within the scope of this standard.

#### 2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 61967 (all parts), *Integrated Circuits – Measurement of electromagnetic emissions, 150 KHz to 1 GHz*

IEC 61967-4, *Integrated circuits – Measurement of electromagnetic emissions, 150 kHz to 1 GHz – Part 4: Measurement of conducted emissions – 1  $\Omega$ /150  $\Omega$  direct coupling method*