# INTERNATIONAL STANDARD

# IEC 61691-3-3

First edition
2001-06

## Behavioural languages –

## Part 3-3:
## Synthesis in VHDL



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INTERNATIONAL ELECTROTECHNICAL COMMISSION

# BEHAVIOURAL LANGUAGES –

## Part 3-3: Synthesis in VHDL

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International Standard IEC 61691-2-3 has been prepared by IEC technical committee 93: Design automation.

This standard is based on IEEE Std 1076-3 (1997: *Synthesis packages*

The text of this standard is based on the following documents:

| FDIS | Report on voting |
|---|---|
| 93/132/FDIS | 93/142/RVD |

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

*This standard does not follow the rules for the structure of international standards given in Part 3 of the ISO/IEC Directives.*

IEC 61691 consists of the following parts, under the general title: *Behavioural languages:*

IEC 61691-1:1997, VHDL language reference manual [1)]

IEC 61691-2:2001, Part 2: VHDL multilogic system for model interoperability

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[1)] The edition 2 with the title: VHSIC hardware description language VHDL (1076a) (under consideration) will replace it.

IEC 61691-3-1, Part 3-1: Analog description in VHDL (under consideration)

IEC 61691-3-2:2001, Part 3-2: Mathematical operation in VHDL

IEC 61691-3-3:2001, Part 3-3: Synthesis in VHDL

IEC 61691-3-4, Part 3-4: Timing expressions in VHDL (under consideration)

IEC 61691-3-5, Part 3-5: Library utilities in VHDL (under consideration)

The committee has decided that the contents of this publication will remain unchanged until 2004. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

# INTRODUCTION

This standard, 61691-3-3, supports the synthesis and verification of hardware designs, by defining vector types for representing signed or unsigned integer values and providing standard interpretations of widely used scalar VHDL values.

This standard includes package bodies, as described in annex A, which are available in electronic format either on a diskette affixed to the back cover, or as a downloadable file from the IEC Web Store.

# BEHAVIOURAL LANGUAGES - Part 3-3: Synthesis in VHDL

## 1. Overview

### 1.1 Scope

This standard defines standard practices for synthesizing binary digital electronic circuits from VHDL source code. It includes the following:

a) The hardware interpretation of values belonging to the BIT and BOOLEAN types defined by IEEE Std 1076-1993[1] and to the STD_ULOGIC type defined by IEEE Std 1164-1993.

b) A function (STD_MATCH) that provides “don’t care” or “wild card” testing of values based on the STD_ULOGIC type.

c) Standard functions for representing sensitivity to the edge of a signal.

d) Two packages that define vector types for representing signed and unsigned arithmetic values, and that define arithmetic, shift, and type conversion operations on those types.

This standard is designed for use with IEEE Std 1076-1993. Modifications that may be made to the packages for use with the previous edition, IEEE Std 1076-1987, are described in 7.2.

[1]Information on references can be found in Clause 2.