INTERNATIONAL STANDARD

IEC 60747-15

First edition 2003-06

Discrete semiconductor devices -

Part 15: Isolated power semiconductor devices

Dispositifs à semiconducteurs -

Partie 15: Dispositifs à semiconducteurs de puissance isolés

© IEC 2003 — Copyright - all rights reserved

No part of this publication may be reproduced or utilized in any form or by any means, electronic or mechanical, including photocopying and microfilm, without permission in writing from the publisher.

International Electrotechnical Commission, 3, rue de Varembé, PO Box 131, CH-1211 Geneva 20, Switzerland Telephone: +41 22 919 02 11 Telefax: +41 22 919 03 00 E-mail: inmail@iec.ch Web: www.iec.ch



CONTENTS

| FO | REW | ORD | 4 |
|------------|---|---|----|
| 1 | Sco | pe | 5 |
| 2 | Norr | native references | 5 |
| 3 | Tern | ns and definitions | 7 |
| 4 | Letter symbols | | |
| | 4.1 | General | |
| | 4.2 | Additional subscripts/symbols | |
| | 4.3 | List letter symbols | |
| 5 | Essential ratings (limiting values) and characteristics | | |
| | 5.1 | General | 13 |
| | 5.2 | Ratings (limiting values) | |
| | 5.3 | Characteristics | |
| 6 | Veri | ication of ratings (limiting values) | 24 |
| | 6.1 | Isolation voltage between terminals and base plate (V_{isol}) | 24 |
| | 6.2 | Peak case non-rupture current | |
| | 6.3 | Maximum terminal current (I _{tRMS}) | 26 |
| | 6.4 | Surge (non-repetitive) current test (I_{FSM} ; I_{TSM}) | 26 |
| 7 | Methods of measurement of characteristics | | |
| | 7.1 | Rated partial discharge inception and extinction voltages (V_i) (V_e) | 26 |
| | 7.2 | Parasitic stray inductance between main terminals (L_{P}) | 27 |
| | 7.3 | Parasitic stray capacitance of functional circuit elements to case (C_P) | |
| | 7.4 | Measuring methods for thermal characteristics | |
| | 7.5 | Measuring methods of mechanical characteristics | |
| 8 | Acce | eptance and reliability | |
| | 8.1 | General requirements | |
| | 8.2 | List of endurance tests | |
| | 8.3 | Type tests and routine tests of isolated power devices | 36 |
| Anı | nex A | (informative) Test method for peak case non-rupture current | 38 |
| Anı | nex B | (informative) Measuring method of the thickness of thermal compound paste | 41 |
| Anı | nex C | (informative) Climatic parameters and characteristics | 42 |
| Anı | nex D | (informative) Internal circuit configurations | 43 |
| Bib | liogra | phy | 44 |
| Eia | uro 1 | Explanation of paracitic industance I | 10 |
| _ | | - Explanation of parasitic inductance L_{P} | |
| | | $-$ Examples for distributed parasitic stray inductances L_{P} | 18 |
| sin | k, wit | a – Example of a cross-section of an isolated power device mounted on a heat n the temperatures $T_{\rm vj},\dots$ $T_{\rm a}$ | 20 |
| Fig res | ure 3 p. Z_{th} | b – Model of thermal resistances of circuit elements $R_{\text{th(j-c)}}$, $R_{\text{th(c-s)}}$, $R_{\text{th(s-a)}}$, $R_{\text{th(s-a)}}$, $R_{\text{th(j-a)}}$, schematically | 20 |
| Fig | ure 4 | – Reference points for measuring the temperatures T_{vj} , T_{c} , T_{cl} , T_{cD} T_{s} to be I for an isolated power device, seen from above | 22 |

| Figure 5 – Transient thermal impedance $Z_{\text{th(j-c)}} = f(t_p)$ of an isolated power semiconductor device as a function of the pulse duration time t_p , elapsed after a step change of applied power dissipation | 23 |
|--|-----|
| Figure 6 – Basic circuit diagram for isolation breakdown with stand voltage test ("high pot test") with $V_{\rm isol}$ | 24 |
| Figure 7 – Isolation levels of an isolated power device with integrated driver and protection functions | 25 |
| Figure 8a – Circuit diagram for measurement of parasitic stray inductances (L_{P}) | 28 |
| Figure 8b – Wave forms | 29 |
| Figure 9 – Circuit for the measurement of parasitic stray capacitance C_{p} of the functional circuit elements to base plate (ground) | 30 |
| Figure 10 – Example for reference points for the measurement of $T_{\rm cref}$ and $T_{\rm sref}$ for the thermal resistance of an isolated power semiconductor devices (dual-switch, 62 mm wide) |)32 |
| Figure 11 – Power cycling (load) capability $N_{\rm f;p}$ versus temperature rise of the junction temperature $T_{\rm vj}$ per load pulse | 34 |
| Figure A.1 – Circuit diagram for test of peak case non-rupture current I_{CNR} | 38 |
| Figure B.1– Example of a measuring gauge for a layer of thermal compound paste of a thickness between 5 μm and 150 μm | 41 |
| Figure D.1 – Converter circuits containing diodes and/or thyristors | 43 |
| Figure D.2 – Inverter circuits containing diodes and/or transistors shown as IGBT | 44 |
| Table 1 – Environmental testing | 35 |
| Table 2 – Minimum type and routine tests for isolated power semiconductor devices | 36 |
| Table C.1 – Classification of climatic environmental conditions, e.g. Class 3K3 and 3K4 (extract, not complete) | 42 |

INTERNATIONAL ELECTROTECHNICAL COMMISSION

DISCRETE SEMICONDUCTOR DEVICES -

Part 15: Isolated power semiconductor devices

FOREWORD

- 1) The IEC (International Electrotechnical Commission) is a worldwide organization for standardization comprising all national electrotechnical committees (IEC National Committees). The object of the IEC is to promote international co-operation on all questions concerning standardization in the electrical and electronic fields. To this end and in addition to other activities, the IEC publishes International Standards. Their preparation is entrusted to technical committees; any IEC National Committee interested in the subject dealt with may participate in this preparatory work. International, governmental and non-governmental organizations liaising with the IEC also participate in this preparation. The IEC collaborates closely with the International Organization for Standardization (ISO) in accordance with conditions determined by agreement between the two organizations.
- 2) The formal decisions or agreements of the IEC on technical matters express, as nearly as possible, an international consensus of opinion on the relevant subjects since each technical committee has representation from all interested National Committees.
- 3) The documents produced have the form of recommendations for international use and are published in the form of standards, technical specifications, technical reports or guides and they are accepted by the National Committees in that sense.
- 4) In order to promote international unification, IEC National Committees undertake to apply IEC International Standards transparently to the maximum extent possible in their national and regional standards. Any divergence between the IEC Standard and the corresponding national or regional standard shall be clearly indicated in the latter.
- 5) The IEC provides no marking procedure to indicate its approval and cannot be rendered responsible for any equipment declared to be in conformity with one of its standards.
- 6) Attention is drawn to the possibility that some of the elements of this International Standard may be the subject of patent rights. The IEC shall not be held responsible for identifying any or all such patent rights.

International Standard IEC 60747-15 has been prepared by subcommittee 47E, Discrete semiconductor devices of IEC technical committee 47: Semiconductor devices

The text of this standard is based on the following documents:

| FDIS | Report on voting |
|--------------|------------------|
| 47E/236/FDIS | 47E/238/RVD |

Full information on the voting for the approval of this standard can be found in the report on voting indicated in the above table.

This publication has been drafted in accordance with the ISO/IEC Directives, Part 2.

The committee has decided that the contents of this publication will remain unchanged until 2006. At this date, the publication will be

- reconfirmed;
- withdrawn;
- replaced by a revised edition, or
- amended.

DISCRETE SEMICONDUCTOR DEVICES -

Part 15: Isolated power semiconductor devices

1 Scope

This part of IEC 60747 gives the product specific standards, requirements and test methods for isolated power semiconductor devices. These requirements are added to those given in other parts of IEC 60747, IEC 60748 and IEC 60749 for the corresponding non-isolated power devices.

2 Normative references

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

IEC 60068-2-6, Environmental testing – Part 2-6: Tests – Test Fc: Vibration (sinusoidal)

IEC 60068-2-7, Environmental testing – Part 2-7: Tests – Test Ga and guidance: Acceleration, steady state

IEC 60068-2-14, Environmental testing – Part 2-14: Tests – Test N: Change of temperature

IEC 60068-2-20, Environmental testing - Part 2-20: Tests - Test T: Soldering

IEC 60068-2-27, Environmental testing – Part 2-27: Tests – Test Ea and guidance: Shock

IEC 60068-2-47, Environmental testing – Part 2-47: Test methods – Mounting of components, equipment and other articles for vibration, impact and other similar dynamic tests

IEC 60068-2-48, Environmental testing – Part 2-48: Test methods – Guidance on the application of the tests of IEC 60068 to simulate the effects of storage

IEC 60068-3-4: Environmental testing – Part 3-4: Supporting documentation and guidance – Damp heat tests

IEC 60191-4:1999, Mechanical standardization of semiconductor devices – Part 4: Coding system and classification into forms of package outlines for semiconductor device packages

IEC 60270:2000, High voltage test techniques – Partial discharge measurements

IEC 60319, Presentation and specification of reliability data for electronic components

IEC 60664-1:1992, Insulation coordination for equipment within low-voltage systems – Principles, requirements and tests

IEC 60721-3-3:1994, Classification of environmental conditions – Part 3-3: Classification of groups of environmental parameters and their severities – Stationary use at weather-protected locations

IEC 60747-1:1983, Semiconductor devices – Discrete devices and integrated circuits – Part 1: General

Amendment 1 (1991)

Amendment 3 (1996)

IEC 60747-2:2000, Semiconductor devices – Discrete devices and integrated circuits – Part 2: Rectifier diodes

IEC 60747-6:2000, Semiconductor devices – Part 6: Thyristors

IEC 60747-7:2000, Semiconductor devices – Part 7: Bipolar transistors

IEC 60747-8:2000, Semiconductor devices – Part 8: Field effect transistors

IEC 60747-9:1998, Semiconductor devices – Discrete devices – Part 9: Insulated-gate bipolar transistors (IGBTs)

IEC 60749-5: Semiconductor devices – Mechanical and climatic test methods – Part 5: Steady-state temperature humidity bias life test

IEC 60749-6: Semiconductor devices – Mechanical and climatic test methods – Part 6: Storage at high temperature

IEC 60749-10: Semiconductor devices – Mechanical and climatic test methods – Part 10: Mechanical shock

IEC 60749-12: Semiconductor devices – Mechanical and climatic test methods – Part 12: Vibration, variable frequency

IEC 60749-14: Semiconductor devices – Mechanical and climatic test methods – Part 14: Robustness of terminations (lead integrity)¹

IEC 60749-15: Semiconductor devices – Mechanical and climatic test methods – Part 15: Resistance to soldering temperature for through-hole mounted devices¹

IEC 60749-21: Semiconductor devices – Mechanical and climatic test methods – Part 21: Solderability¹

IEC 60749-25: Semiconductor devices – Mechanical and climatic test methods – Part 25: Rapid change of temperature (air, air)¹

IEC 60749-26: Semiconductor devices – Mechanical and climatic test methods – Part 26: Rapid change of temperature (air, air)¹

IEC 60749-36: Semiconductor devices – Mechanical and climatic test methods – Part 36: Acceleration, steady-state

IEC 61287-1:1995, Power convertors installed on board rolling stock – Part 1: Characteristics and test methods²

ISO 1302:2002, Geometrical Product Specifications (GPS) – Indication of surface texture in technical product documentation

ISO 2768-2:1989, General tolerances – Part 2: Geometrical tolerances for features without individual tolerance indications

¹ In preparation.

² A new edition is being prepared.